MCR08BT1

SCR

Rev.02 - 25 February 2025 Product data sheet

1. General description

Planar passivated SCR with sensitive gate in a SOT223 surface mountable plastic package. This SCR is designed to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

2. Features and benefits

- Sensitive gate
- Planar passivated for voltage ruggedness and reliability
- Direct triggering from low power drivers and logic ICs
- Surface mountable package

3. Applications

- General purpose switching and phase control
- Ignition circuits, CDI for 2- and 3-wheelers
- Motor control - e.g. small kitchen appliances

4. Quick reference data

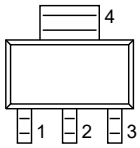
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{RRM}	repetitive peak reverse voltage			-	-	200	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{sp} \leq$ 112 °C; Fig. 1		-	-	0.5	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{sp} \leq$ 112 °C; Fig. 2; Fig. 3		-	-	0.8	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)}$ = 25 °C; t_p = 10 ms; Fig. 4; Fig. 5		-	-	8	A
		half sine wave; $T_{j(init)}$ = 25 °C; t_p = 8.3 ms		-	-	9	A
T_j	junction temperature			-	-	125	°C
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 10 mA; T_j = 25 °C; Fig. 9		-	50	200	µA
Dynamic charateristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 134 V; T_j = 125 °C; R_{GK} = 1 kΩ; (V_{DM} = 67% of V_{DRM}); exponential waveform; Fig. 14		500	800	-	V/µs

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		V_{DM} = 134 V; T_j = 125 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit; Fig. 14		-	25	-	V/µs

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K	cathode	 SC-73 (SOT223)	
2	A	anode		
3	G	gate		
4	A	mb; connected to anode		

6. Ordering information

Table 3. Ordering information

Type number	Package Name	Orderable part number	Packing method	Small packing quantity	Package version	Package issue date
MCR08BT1	SOT223	MCR08BT1, 115	Reel	1000	SOT223	16-Mar-2006

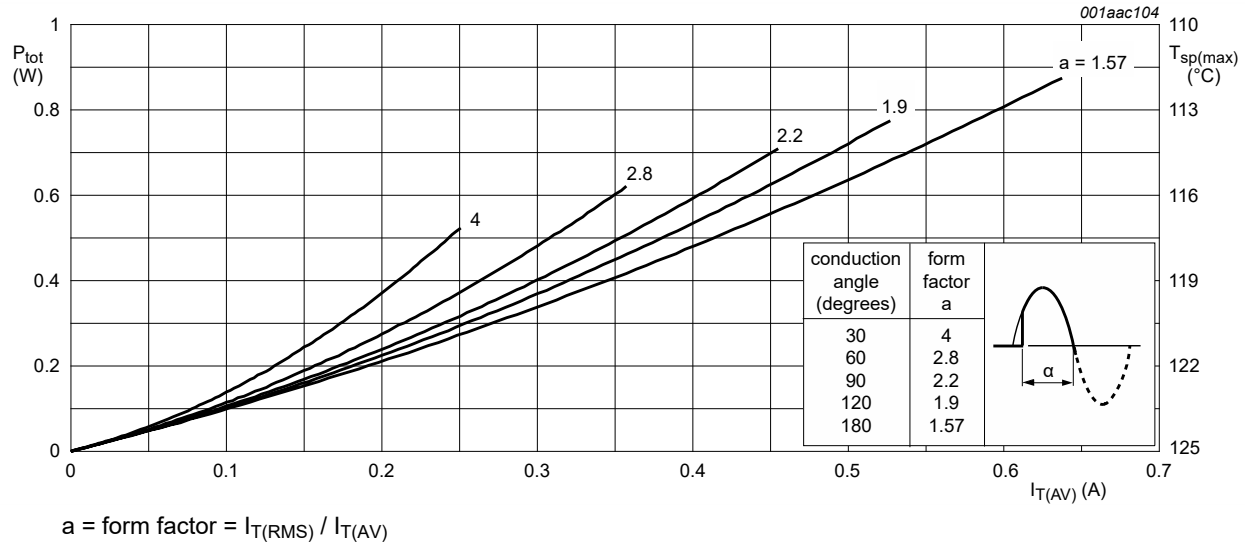
Type number	Marking codes	
	Assembly factory: d	Assembly factory: L
MCR08BT1	Jdxxx CR08B	JLxxx CR08B

7. Limiting values

Table 4. Limiting values

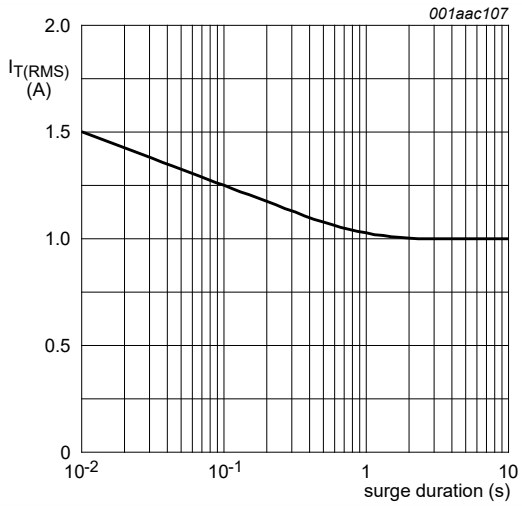
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage			-	200	V
V_{RRM}	repetitive peak reverse voltage			-	200	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{sp} \leq$ 112 °C; Fig. 1		-	0.5	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{sp} \leq$ 112 °C; Fig. 2; Fig. 3		-	0.8	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)}$ = 25 °C; t_p = 10 ms; Fig. 4; Fig. 5		-	8	A
		half sine wave; $T_{j(init)}$ = 25 °C; t_p = 8.3 ms		-	9	A
I^2t	I^2t for fusing	t_p = 10 ms; SIN		-	0.32	A²s
dI_T/dt	rate of rise of on-state current	I_T = 2 A; I_G = 10 mA; dI_G/dt = 100 mA/µs		-	50	A/µs
I_{GM}	peak gate current			-	1	A
V_{RGM}	peak reverse gate voltage			-	5	V
P_{GM}	peak gate power			-	2	W
$P_{G(AV)}$	average gate power	over any 20 ms period		-	0.1	W
T_{stg}	storage temperature			-40	150	°C
T_j	junction temperature			-	125	°C



a = form factor = $I_{T(RMS)}$ / $I_{T(AV)}$

Fig. 1. Total power dissipation as a function of average on-state current; maximum values



f = 50 Hz; T_{sp} = 112 °C

Fig. 2. RMS on-state current as a function of surge duration for sinusoidal currents; maximum values

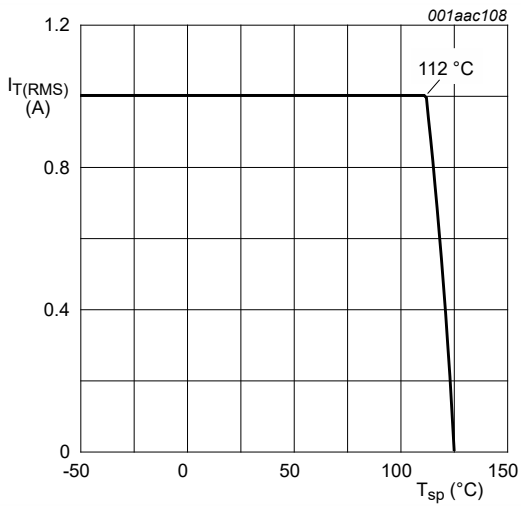
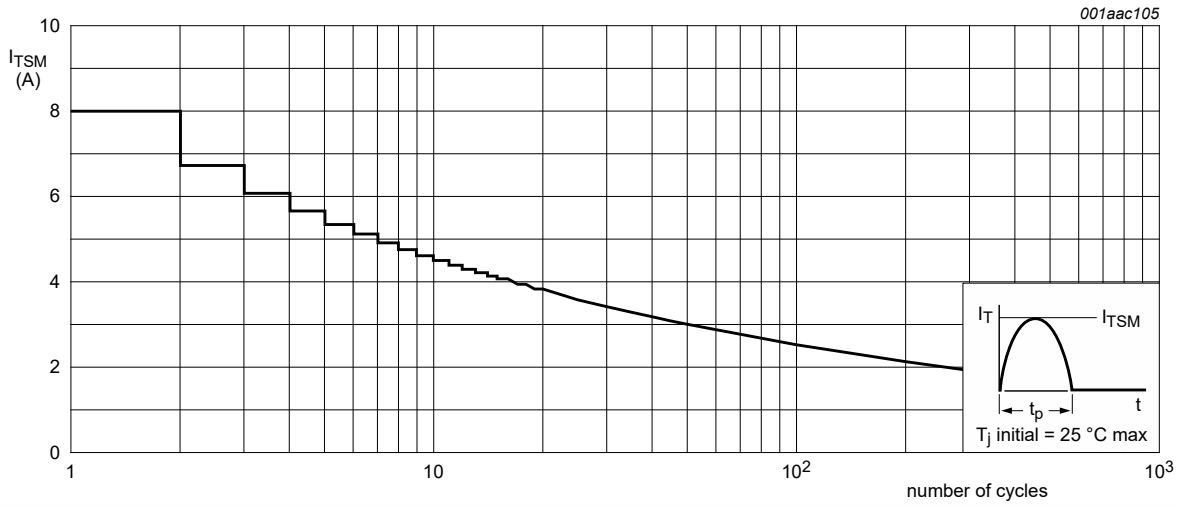


Fig. 3. RMS on-state current as a function of solder point temperature; maximum values



f = 50 Hz

Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

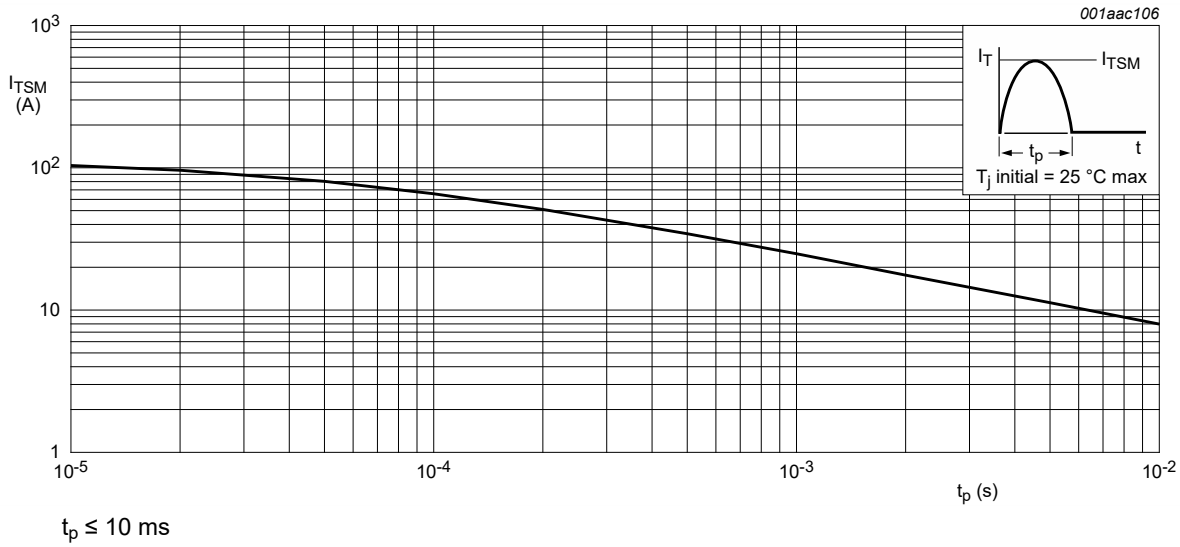


Fig. 5. Non-repetitive peak on-state current as a function of pulse width for sinusoidal currents; maximum values

8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	Fig. 6		-	-	15	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	printed circuit board mounted; minimum pad area; in free air; Fig. 7		-	70	-	K/W
		printed circuit board mounted; minimum footprint; in free air; Fig. 8		-	156	-	K/W

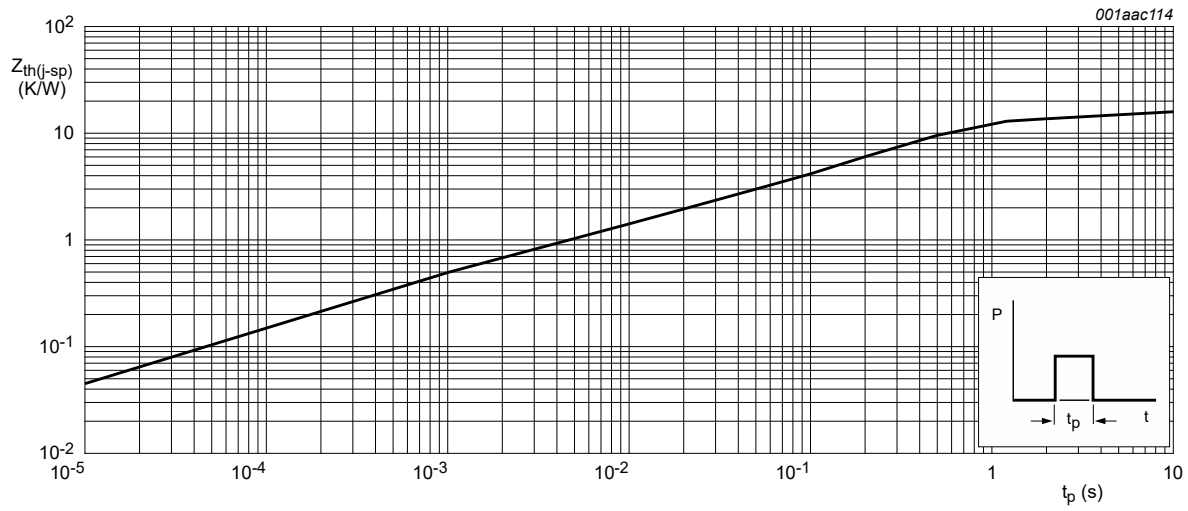
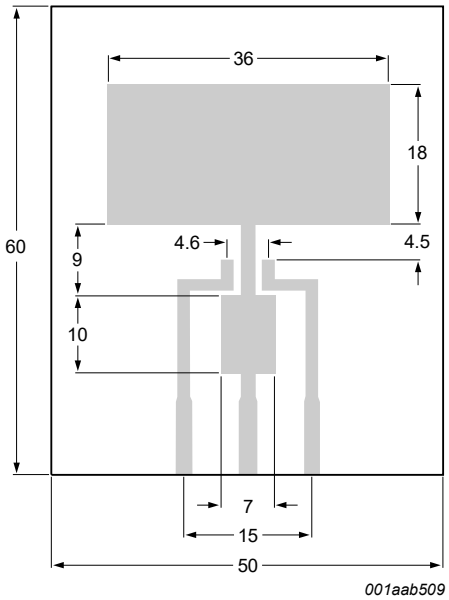
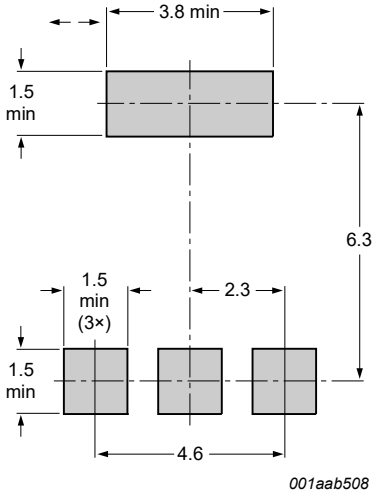


Fig. 6. Transient thermal impedance from junction to solder point as a function of pulse duration



All dimensions are in mm
Printed circuit board:
FR4 epoxy glass (1.6 mm thick), copper laminate (35 um thick)

Fig. 7. Printed circuit board pad area: SOT223



All dimensions are in mm

Fig. 8. Minimum footprint SOT223

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 10 mA; T_j = 25 °C; Fig. 9		-	50	200	µA
I_L	latching current	V_D = 12 V; I_G = 0.5 mA; T_j = 25 °C; $R_{GK(ext)}$ = 1 kΩ; Fig. 10		-	2	6	mA
I_H	holding current	V_D = 12 V; T_j = 25 °C; $R_{GK(ext)}$ = 1 kΩ; Fig. 11		-	2	5	mA
V_T	on-state voltage	I_T = 1.2 A; T_j = 25 °C; Fig. 12		-	1.25	1.7	V
V_{GT}	gate trigger voltage	V_D = 12 V; I_T = 10 mA; T_j = 25 °C; Fig. 13		-	0.5	0.8	V
		V_D = 200 V; I_T = 10 mA; T_j = 125 °C; Fig. 13		0.2	0.3	-	V
I_D	off-state current	V_D = 200 V; $R_{GK(ext)}$ = 1 kΩ; T_j = 125 °C		-	0.05	1	mA
I_R	reverse current	V_R = 200 V; T_j = 125 °C; $R_{GK(ext)}$ = 1 kΩ		-	0.05	1	mA
Dynamic charateristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 134 V; T_j = 125 °C; R_{GK} = 1 kΩ; (V_{DM} = 67% of V_{DRM}); exponential waveform; Fig. 14		500	800	-	V/µs
		V_{DM} = 134 V; T_j = 125 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit; Fig. 14		-	25	-	V/µs
t_{gt}	gate-controlled turn-on time	I_{TM} = 2 A; V_D = 200 V; I_G = 10 mA; dI_G/dt = 0.1 A/µs; T_j = 25 °C		-	2	-	µs
t_q	commutated turn-off time	V_{DM} = 134 V; T_j = 125 °C; I_{TM} = 1.6 A; V_R = 35 V; $(dI_T/dt)_M$ = 30 A/µs; dV_D/dt = 2 V/µs; $R_{GK(ext)}$ = 1 kΩ; (V_{DM} = 67% of V_{DRM})		-	100	-	µs

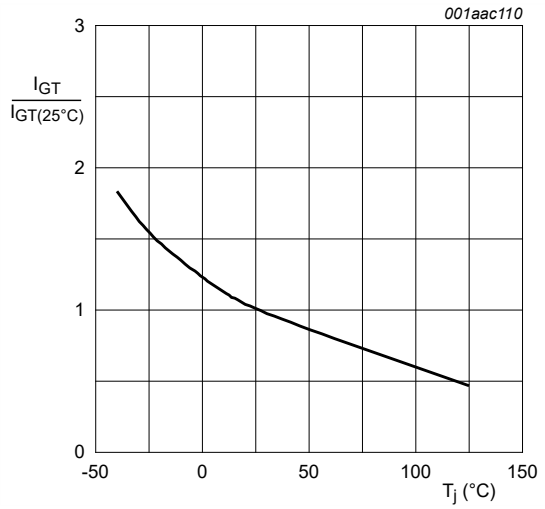
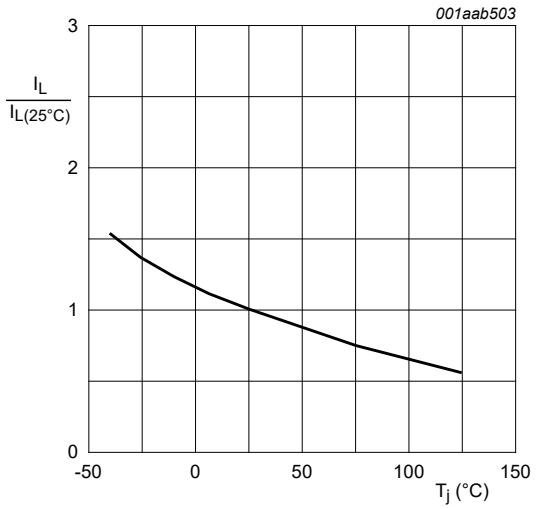
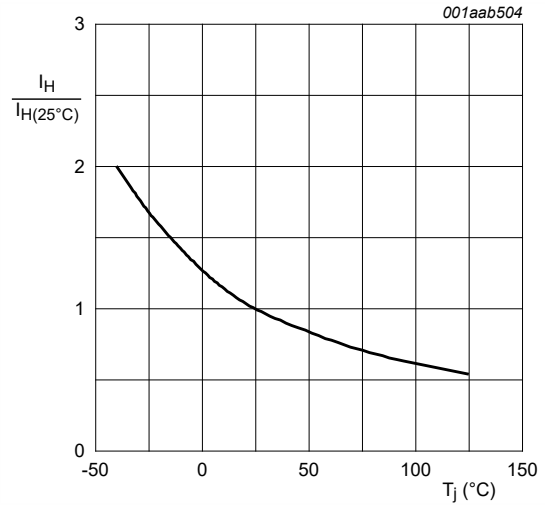


Fig. 9. Normalized gate trigger current as a function of junction temperature



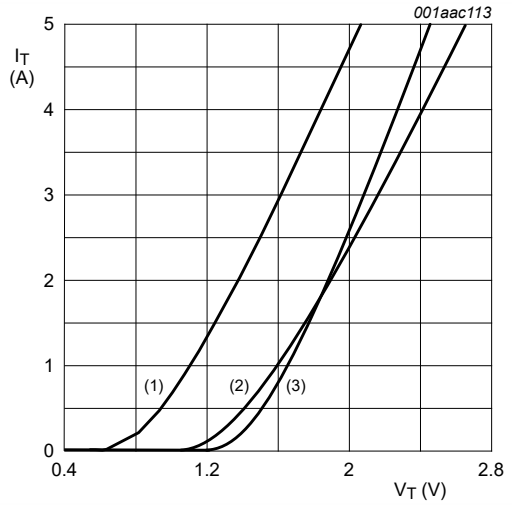
R_{GK} = 1 kΩ

Fig. 10. Normalized latching current as a function of junction temperature



R_{GK} = 1 kΩ

Fig. 11. Normalized holding current as a function of junction temperature



V_o = 1.0 V; R_s = 0.27 Ω
(1) T_j = 125 °C; typical values
(2) T_j = 125 °C; maximum values
(3) T_j = 25 °C; maximum values

Fig. 12. On-state current as a function of on-state voltage

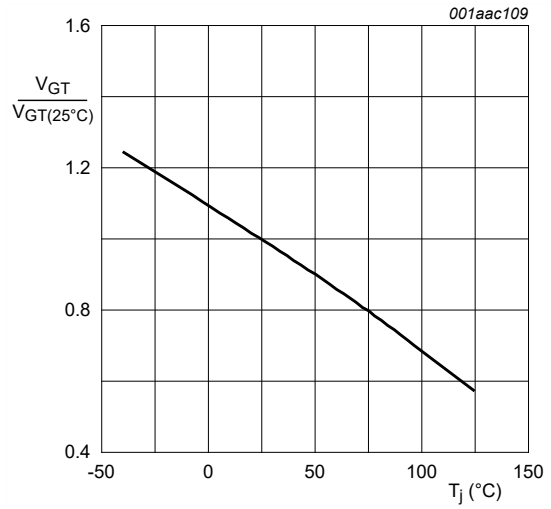
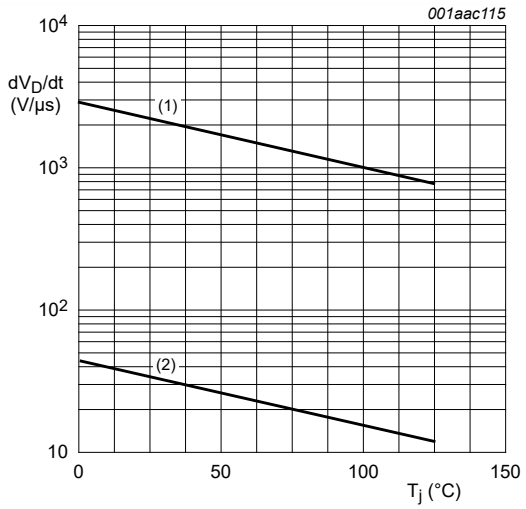


Fig. 13. Normalized gate trigger voltage as a function of junction temperature

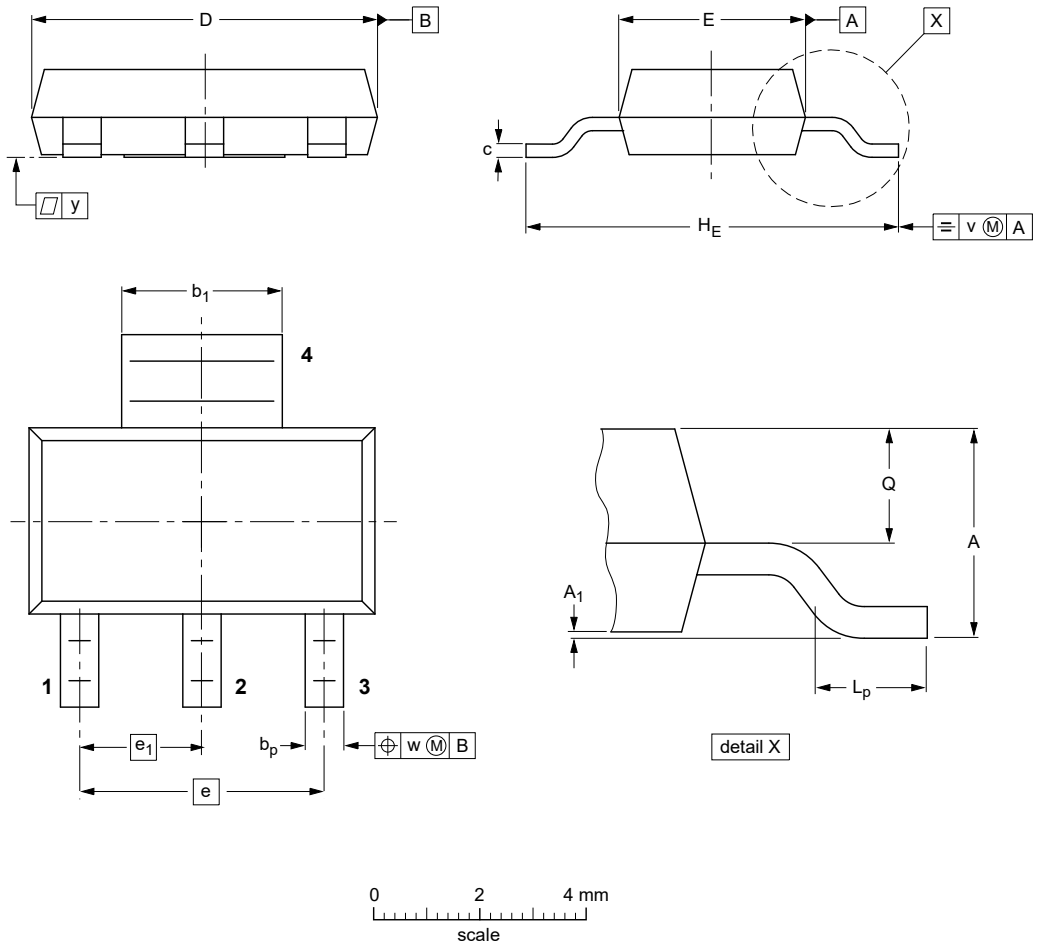


(1) R_{GK} = 1 kΩ
(2) Gate open circuit

Fig. 14. Critical rate of rise of off-state voltage as a function of junction temperature; typical values

10. Package outline

Plastic surface-mounted package with increased heatsink; 4 leads **SOT223**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.8 1.5	0.10 0.01	0.80 0.60	3.1 2.9	0.32 0.22	6.7 6.3	3.7 3.3	4.6	2.3	7.3 6.7	1.1 0.7	0.95 0.85	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT223			SC-73			~~04-11-10~~ 06-03-16

Fig. 15. Package outline SC-73 (SOT223)

11. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".
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